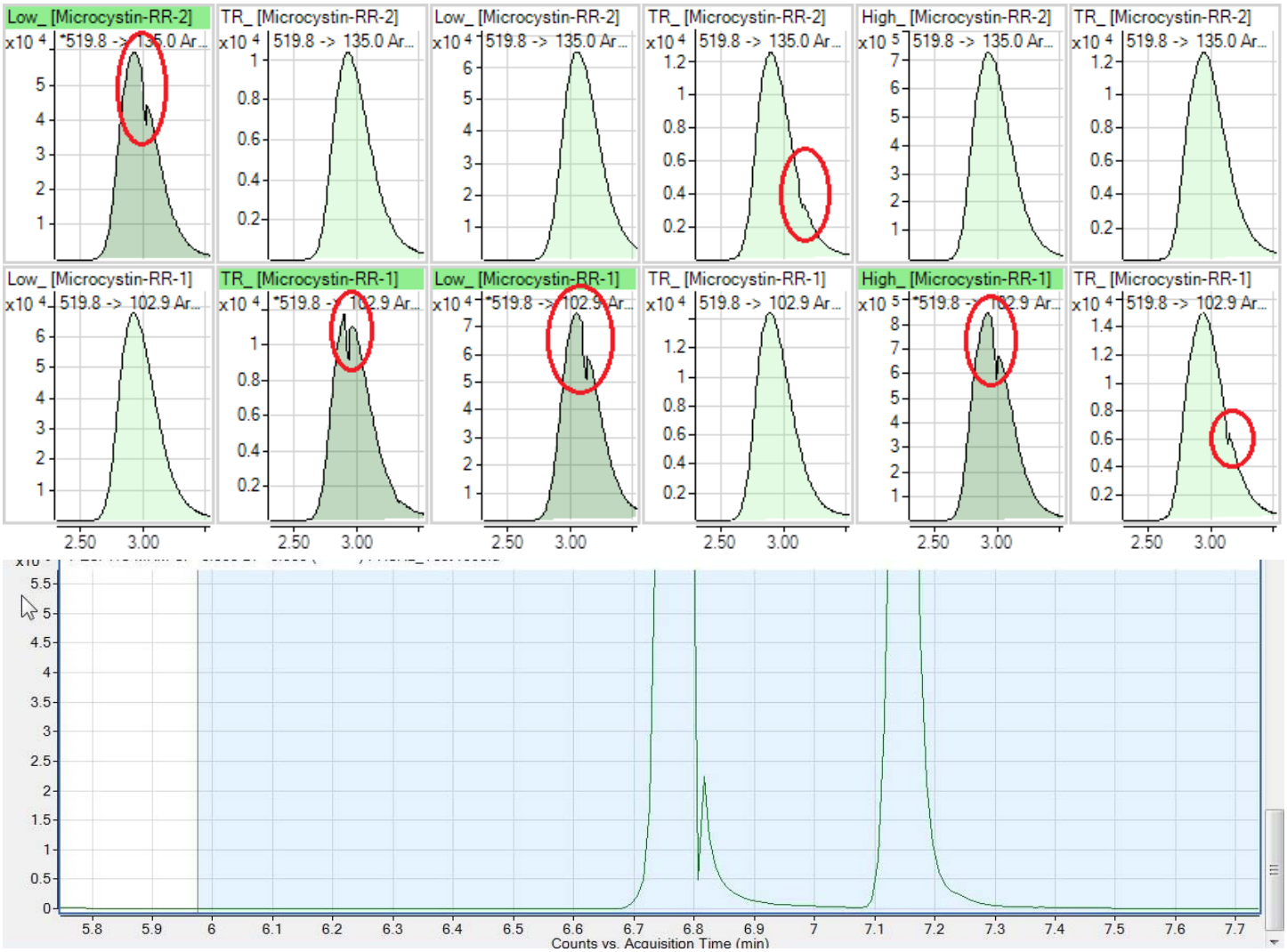
FPGA Update Tool - Instruction

Agilent Technologies

Situation and Explanation: Reports of "distorted chromatographic peaks" was resolved by updating the Mainboard FPGA version to 0x24. This FPGA Update Tool is for Agilent LCMS QQQ, G6400 series, with mainboard part number G7000-65105/61105 only – check the mainboard part number. The update tool's algorithm checks mainboard's FPGA version and will proceed the update if mainboard FPGA version is 0x24 or older. The tool will ignore 0x25 and later.



Description of correction for data dropout problem

"When MRM transitions are made that change collision energy, the electrical potentials in elements prior to the collision cell are modified to achieve the desired collision energy. Due to a problem in the FPGA (Field Programmable Gate Array) logic on the system's Main Board, occasionally two of the potentials that set the collision energy can be left at their previous values because of a transition, resulting in collision energy different that is desired.

The reason why this happens is due to how the voltages are set. The voltages are set using a serial Digital to Analog Converter (DAC) with multiple outputs. The embedded control processor of the system sends the voltage settings to the main board in parallel fashion. These setting are converted to serial streams by the FPGA. Because it takes some time to

send the serial steam to the DAC the settings are placed in a First in First Out (FIFO) memory while they are being written. The FIFO is implemented as a circular buffer where two pointers are incremented or decremented as information is written to or read from the memory. A comparator that looks at the pointers is used by DAC writing logic to determine whether there are values that need to be written. Because it takes a finite amount of time for the FIFO pointers to change their values, we determined that an extra glitch can appear on the comparator that on certain rare occasions causes the logic that writes to the DACs to not update properly. A gate has been added to the DAC writing logic to eliminate the glitches that would cause the DACs not to be written.

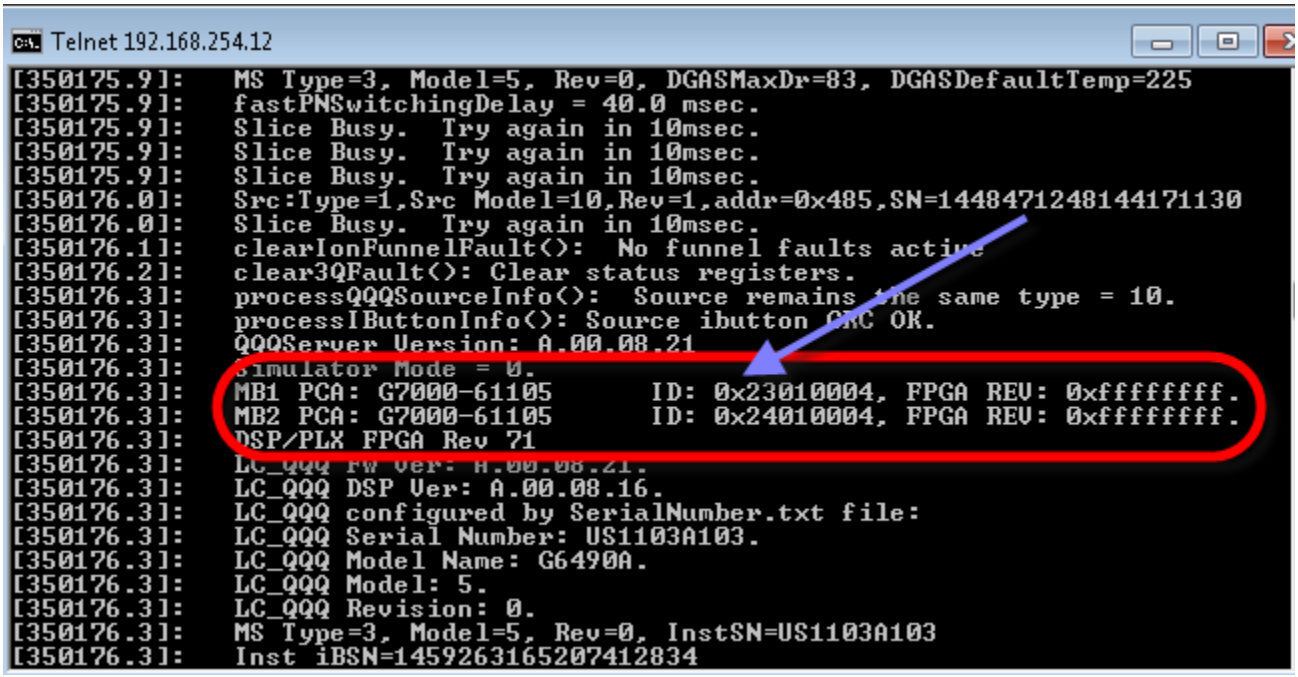
We have extensively tested the FPGA logic change on multiple systems both to be sure that the drop outs are eliminated and to be sure that no unintended artifacts result. We have run the pesticide method from Japan on multiple systems as long as four days without seeing any dropouts. We have run on systems for days using methods developed to induce dropouts every few minutes, and have seen no dropouts. We have also run a series of “regression” tests used by our software team to check various elements of system functionally and have not seen any unexpected artifacts.”

Process: “To be performed ONLY by LCMS QQQ Trained Field Service Engineer”

Download a copy of the FPGA Update Program - QQQ_0x24_FPGA_Uploader.zip – from the Support Portal. Unzip and copy this in a temp directory in the PC (connected to the QQQ).

Please follow the procedure below:

A. Mainboard FPGA Version
   a. Open ‘backdoor’ with telnet
   b. Type ‘get3qverinfo’
   c. Example screenshot below:

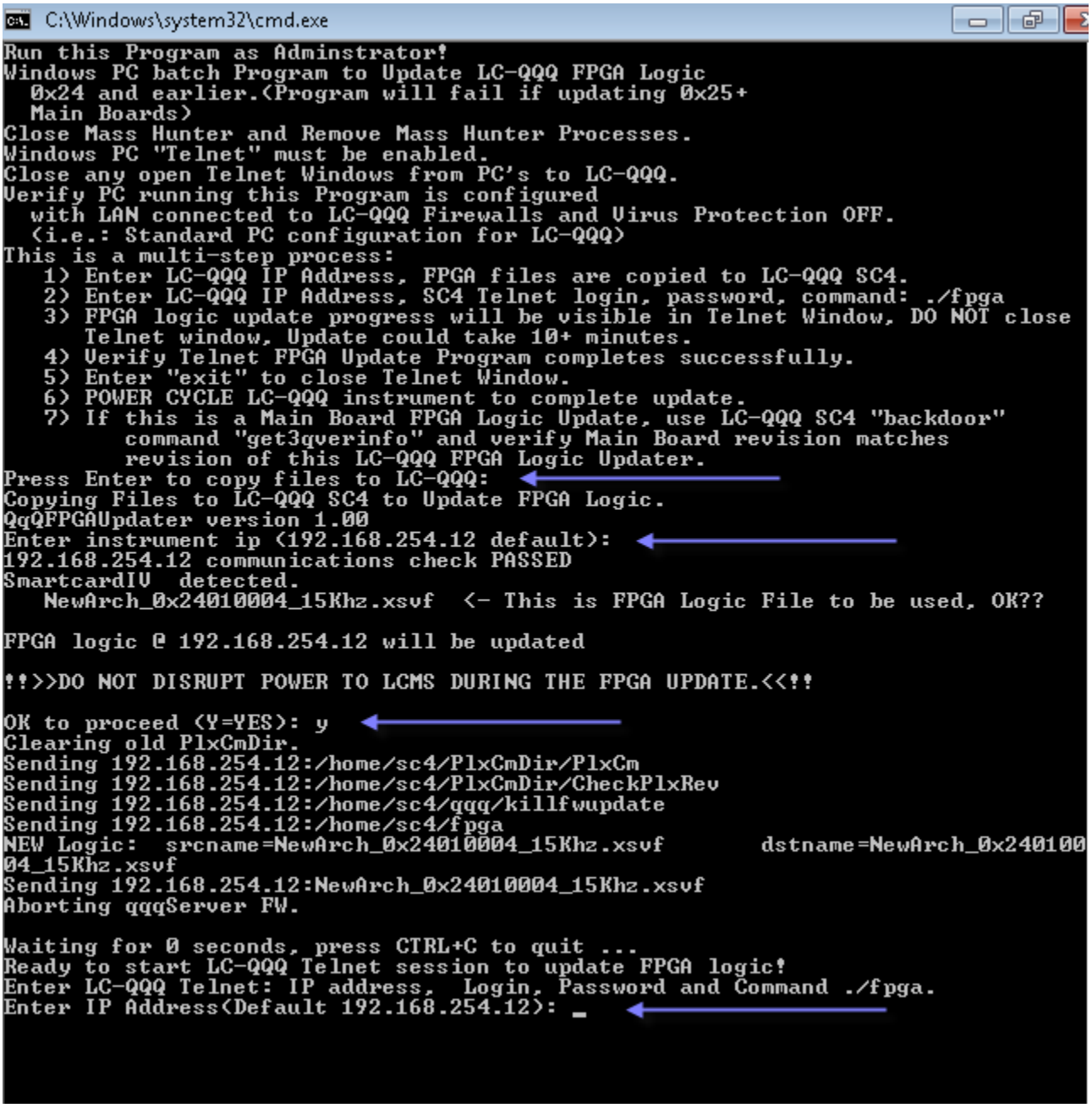


In this example above: MB1 PCA is 0x23, MB2 PCA is 0x24

B. FPGA Upload Process:

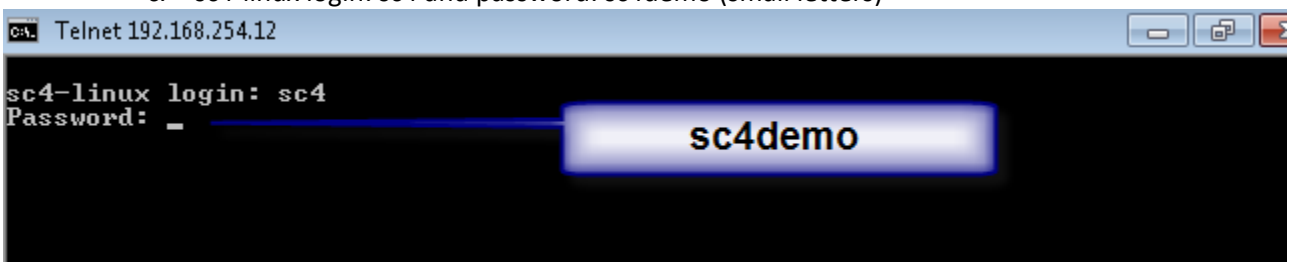
a. Using Windows Explorer, execute QQQ_0x24_FPGA_Uploader.exe (‘Run as Administrator’)

b. Please see below:

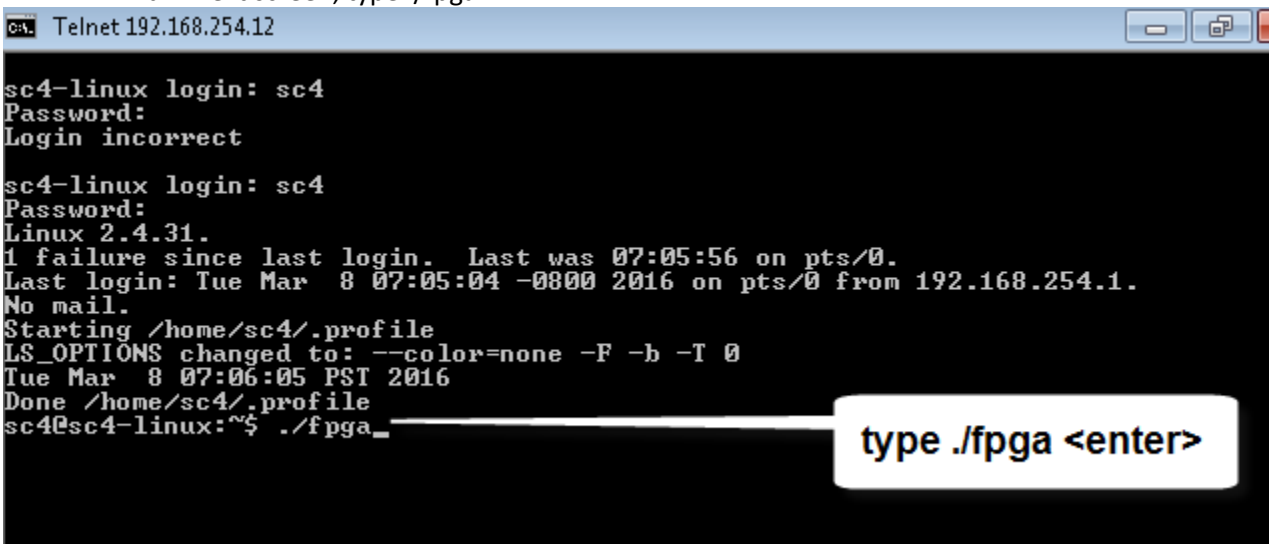


Above, follow the instruction.

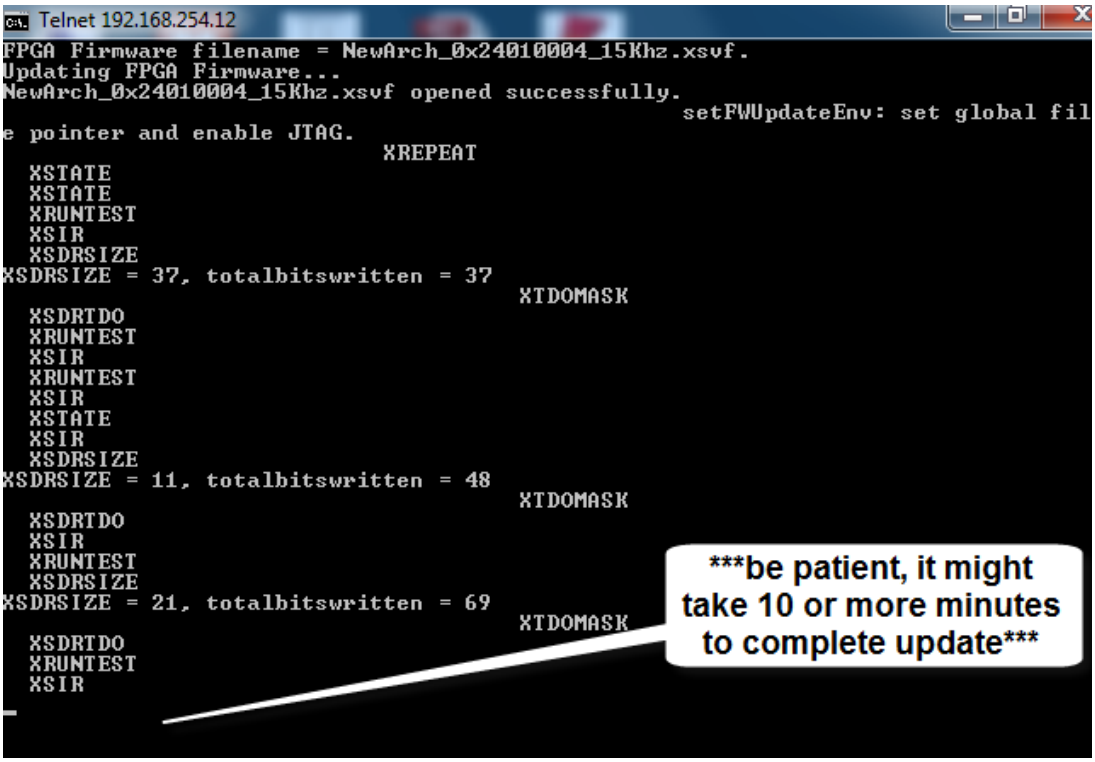
c. sc4-linux login: sc4 and password: sc4demo (small letters)



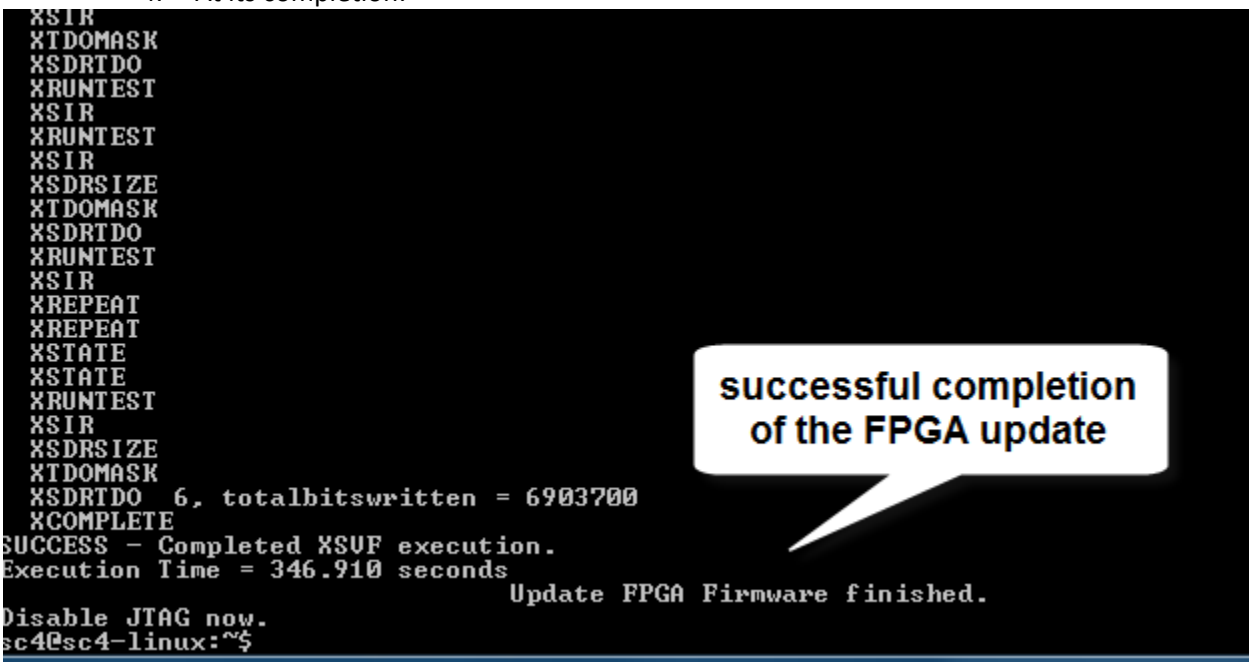
d. next screen, type ./fpga



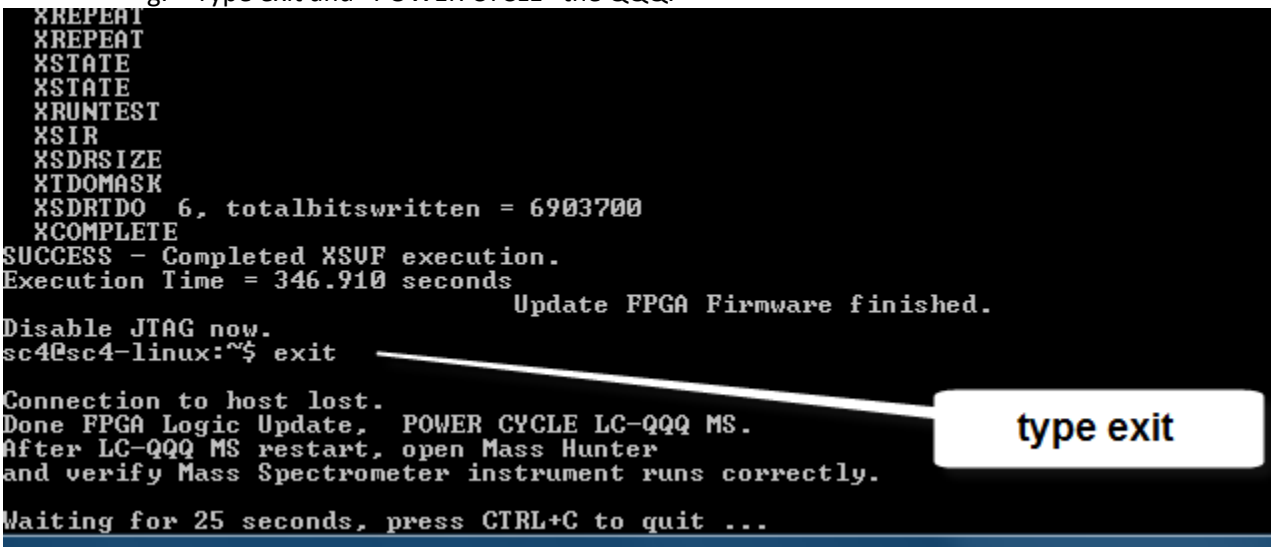
e. You should see below:



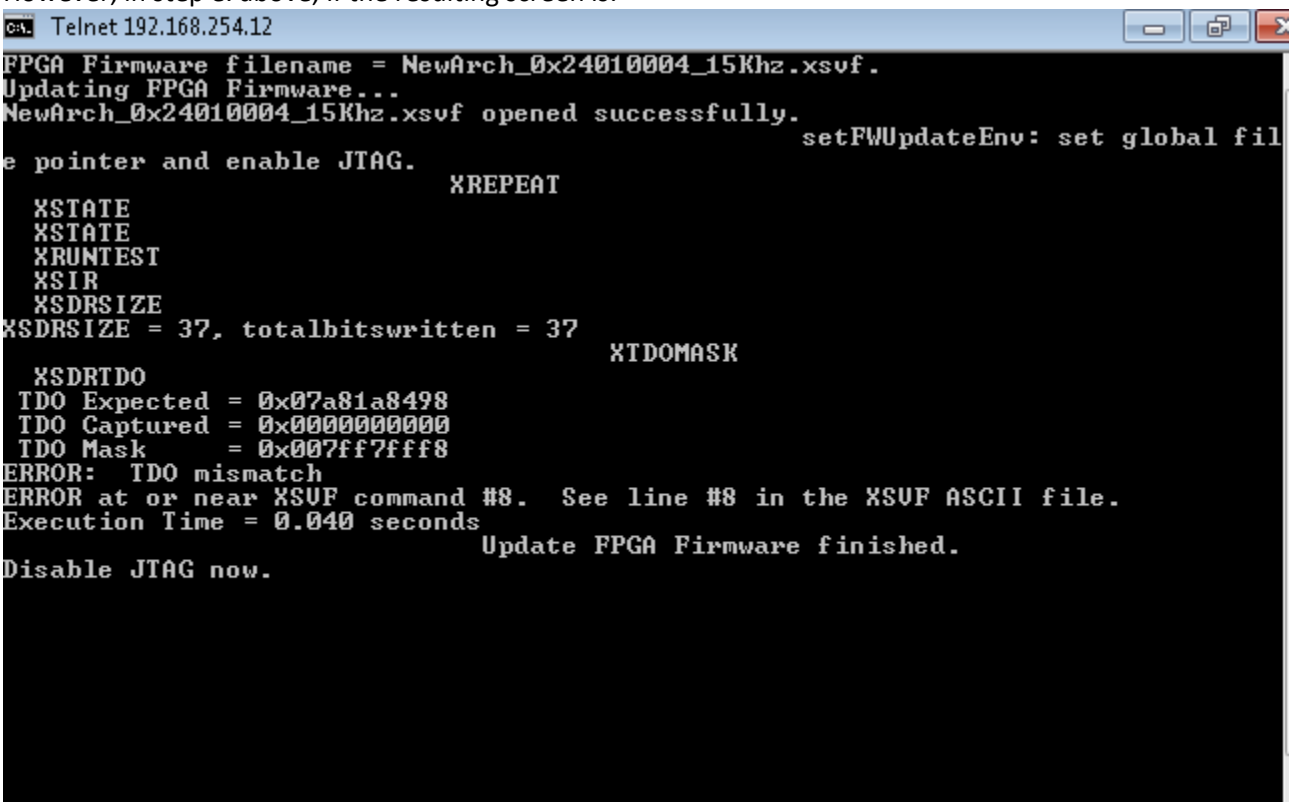
f. At its completion:



g. Type exit and “POWER CYCLE” the QQQ.

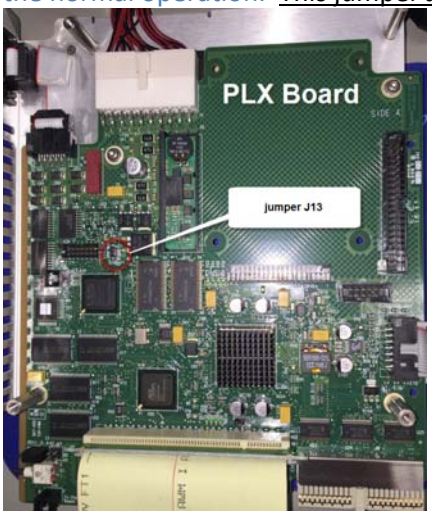


However, in step e. above, if the resulting screen is:



Unfortunately, the uploader did NOT complete its purpose of updating the mainboard's FPGA.

Background Information: The PLX board (pictured below) has a jumper J13 that needs to be set correctly for the FPGA uploader program to work correctly. That jumper is part of the JTAG chain. The only purpose of that JTAG chain is to program the FPGAs. There are 3 devices in this specific JTAG chain: FPGA on the PLX board, FPGA on the main board 1 and FPGA on the main board 2. In some cases, such as the simulator used by software developer, there is no main board, so the JTAG chain is broken. The jumper is a way to loop back the JTAG signal in absence of the main board. These jumps (include the ones on the main board) are only used when updating the FPGA bits. They have no effect on the normal operation. This jumper J13 on the PLX board has to be set to 'Global' position. See pictures below:



Next steps to follow:

1. Install Vacuum Keep Alive Switch Box (part number 1960-67001)
2. Turn off front switch
3. Remove smartcard kit (smartcard with PLX board) from card cage
4. Remove smartcard PCA from the kit
5. Check jumper J13 on PLX board and switch jumper from 'local' to 'global' position

6. Re-install smartcard, smartcard kit back to card cage
7. Turn power back on
8. Remove Vacuum Keep Alive Switch Box
9. QQQ will complete smartcard initialization, wait 5 minutes
10. Go back to Step B, above, FPGA Upload Process
11. After successful FPGA upload, re-verify by performing Step A, above, Mainboard FPGA Version